NEW VERSATILE MODEL: ACCURATE PREDICTION AND SYNTHESIS ABILITY FOR ARBITRARY GEOMETRY FET

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ABSTRACT

An original transistor modeling and synthesis approach, using electromagnetic simulation, is successfully used to describe various FET response.

Starting from one single sample, this novel method can predict numerous other device response, which can strongly differ in geometry and gate width. This model shows excellent agreement with experimental data.

Other papers [1] [2] have been published on active circuit electromagnetic analysis but, we propose and demonstrate, for the first time, synthesis ability.

I INTRODUCTION

In MMICs development, cost and time reduction is a critical issue. Low development costs require MMICs performance to meet specifications at the first pass. This success can only be achieved if powerful CAD tool and accurate models are available. Electromagnetic (EM) softwares are one of these modern tools which are more and more used for industrial designs [3] [4].

Now, one sample transistor measurement can only provide one model. Classic scaling rules [5], on the entire device, are not enough accurate and can not provide reliable extrapolated model. Geometric parameters (finger number, gate width, electrodes layout, ...) are limited by available transistor samples. Designers have then to choose between extensive measurements and modeling and a reduce model choice. Systematic modeling is time consuming and not cost effective. A reduce model choice brings technical limitations and does not allow DC power consumption, chip size and electrical response optimizations.

To overcome this dilemma, we propose an original modeling and synthesis approach using EM simulations of electrodes and intrinsic finger electrical equivalent model.

II NEW MODEL CONCEPT

The transistor model is divided in a passive part, a [S] matrix corresponding to the metallic electrodes response, connected with "n" identical equivalent schemes modeling the "n" finger semiconductor electrical behavior, [Fig.1].

A standard Π model equivalent circuit is used to model the intrinsic active finger electrical response, [Fig.2].

The whole metallic network is simulated with an EM software, Momentum from HP-EEsof. This EM simulation gives an [S] matrix. This matrix takes into account both extrinsic access resistances, capacitances and inductances and also connection lines. In order to connect the EM resulting [S] matrix with the active finger models, the EM input layout contains internal ports in each gate, drain and source electrodes of the transistor, [Fig.3].

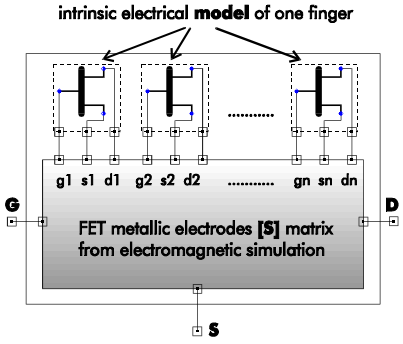

Fig.1: *proposed model for a complete multi-finger transistor*

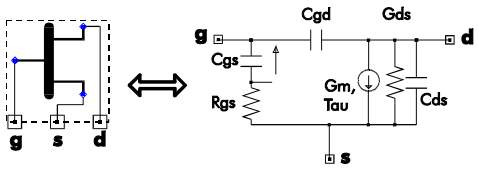

Fig.2: *intrinsic equivalent model of the active finger*

III PREDICTION ABILITY

Metallic layout and active finger are separately known. Thus, the transitor layout can be separately optimized without any geometrical limitation. To predict a new transistor response, we only need to simulate new metallic electrodes and to connect the [S] matrix with "m" finger identical intrinsic model already known. This is a significant progress for MMIC designers as, from now on, they can use transistors they really need. Their choice is no more limited in devices already saved in database. It is now possible to indeed choose finger number, total gate development but also electrodes geometry to optimize the MMIC performances without active device model ability problem.

The new model prediction shows a good agreement with measures and just requires one multibiasing measurement : starting from a U-shape (interdigited) Nstart x Wstart, e.g. U-shape 2x50µm, it can predict every other transistor size like U-shape Npredicted x Wstart, e.g. U-shape 6x50µm. Starting from the same sample measurement, a U-shape Nstart x Wstart, it can model a T-shape Npredicted x Wstart, e.g. T-shape 2x50µm. The new model can also predict gate width changes like Npredicted x Wpredicted using classic scaling rules but applied only to the elementary fingers. In addition, internal ports can be introduced along the transistor electrodes to take into account the propagation effects.

IV EXTRACTION METHODOLOGY

In order to extract the circuit models we need two sets of parameters. First, [S] parameters of the unique sample device have to be measured for few biasing conditions [Vds, Vgs].

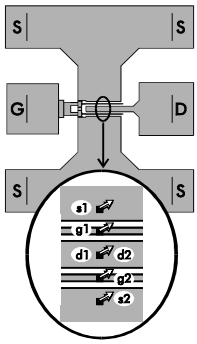

Fig.3: *Sample U-shape 2x50µm measured to model intrinsic finger*

Secondly, an EM simulation of all transistor metallic parts is performed and allows to generate an [S] matrix.

Identical finger intrinsic models, connected with the passive part [S] matrix, are simultaneously optimized to fit the complete transistor measurement for different bias conditions, [Fig.4].

Then the elementary finger equivalent scheme can be connected with any other new metallic electrodes to predict and synthesize a new active device, [Fig.4].

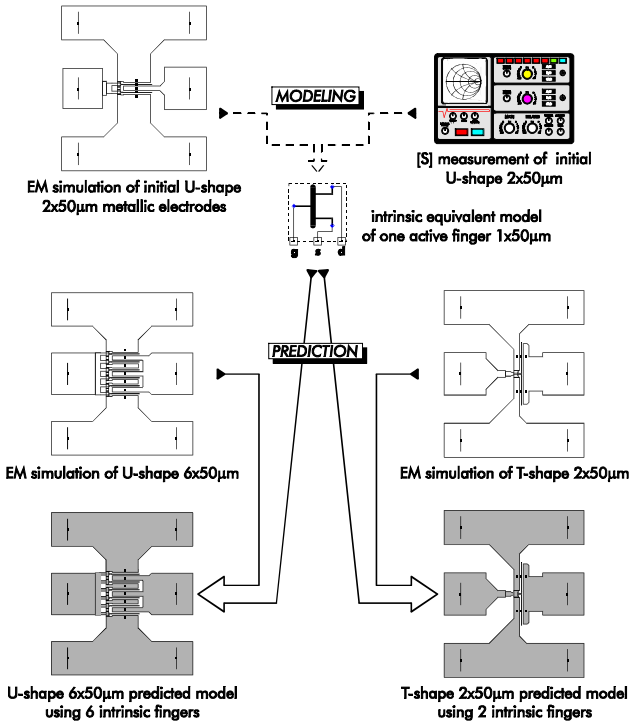

Fig.4: *novel approach synopsis*

V RESULTS AND VALIDATION

To demonstrate the validity of our approach, we present comparisons between measured [S] parameters and modeled [S] parameters.

In this paper we only present comparisons for Vds=3V and Idss/2 but we have observed the same accuracy with Vds=3V and Vgs from –1.8V to 0.4V.

Charts concerning our starting transistor, a U-shape 2x50µm, are in [Fig.5] and [Fig.6]. We also produce equivalent circuit parameters values for the 1x50µm intrinsic finger in [Fig.7] thru [Fig.10] and in [Tab.1].

The proposed modeling method has been applied to 0.2µm PHEMT from Philips Microwave Limeil, FRANCE.

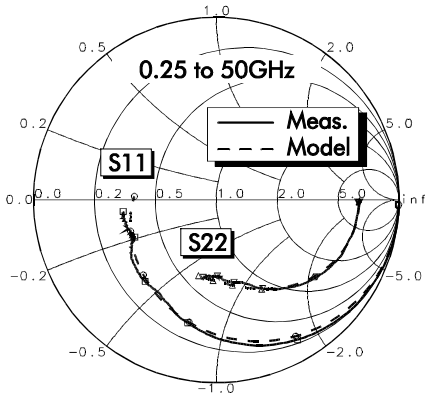

Fig.5: *comparison between measured and modeled [S] parameters of a U-shape 2x50µm biased at Vds=3V and Idss/2*

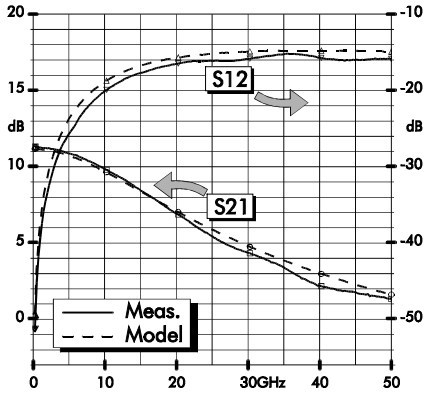

Fig.6: *comparison between measured and modeled [S] parameters of a U shape 2x50µm biased at Vds=3V and Idss/2*

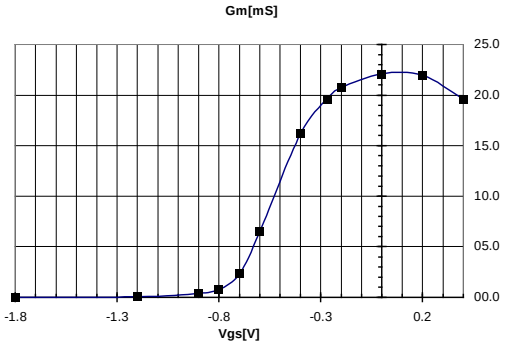

Fig.7: *Equivalent circuit transconductance as a function of Vgs for 1x50µm intrinsic finger biased at Vds=3V*

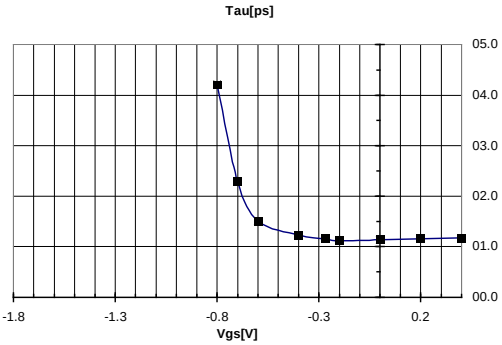

Fig.8: *Equivalent circuit time delay as a function of Vgs for 1x50µm intrinsic finger biased at Vds=3V*

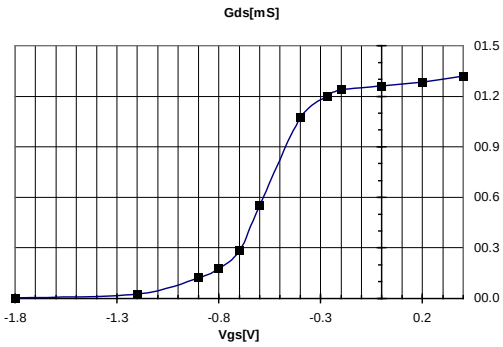

Fig.9: *Equivalent circuit Drain-Source conductance as a function of Vgs for 1x50µm intrinsic finger biased at Vds=3V*

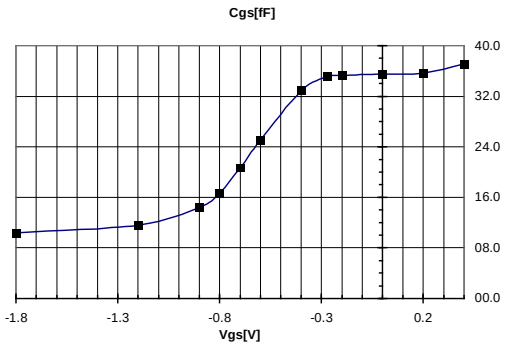

Fig.10: *Equivalent circuit Gate-Source capacitance as a function of Vgs for 1x50µm intrinsic finger biased at Vds=3V*

Rgs [Ω]	Cgd [fF]	Cds [fF]
7.7	6.9	4.0

Tab.1: *Vgs-independent equivalent circuit parameters for 1x50µm intrinsic finger biased at Vds=3V*

To estimate the proposed approach prediction ability, we present comparisons between measured [S] parameters and predicted [S] parameters. [Fig.11] and [Fig.12] show charts concerning a predicted U-shape 6x50µm. Charts concerning a predicted T-shape 2x50µm are in [Fig.13] and [Fig.14].

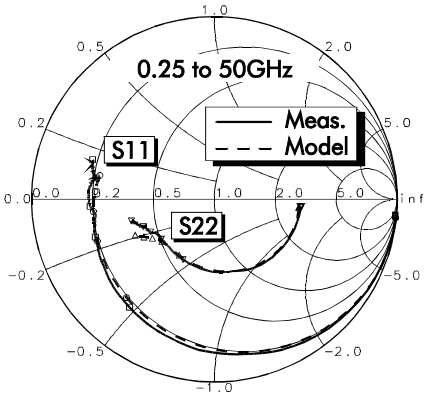

Fig.11: *comparison between measured and predicted [S] parameters of a U-shape 6x50µm biased at Vds=3V and Idss/2*

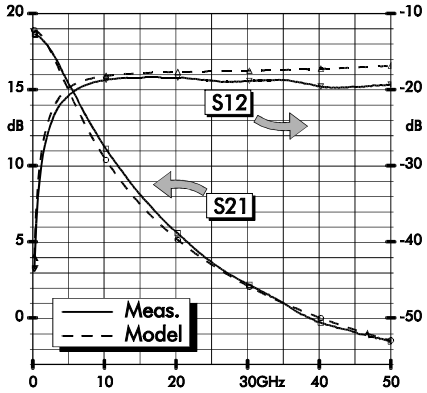

Fig.12: *comparison between measured and predicted [S] parameters of a U-shape 6x50µm biased at Vds=3V and Idss/2*

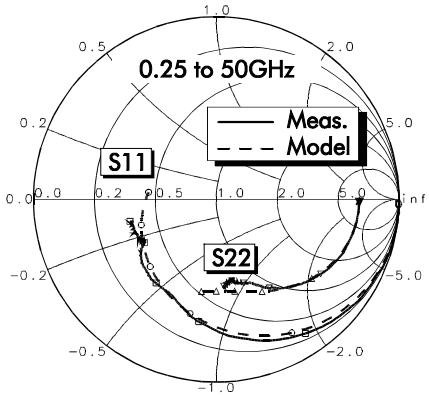

Fig.13: *comparison between measured and predicted [S] parameters of a T-shape 2x50µm biased at Vds=3V and Idss/2*

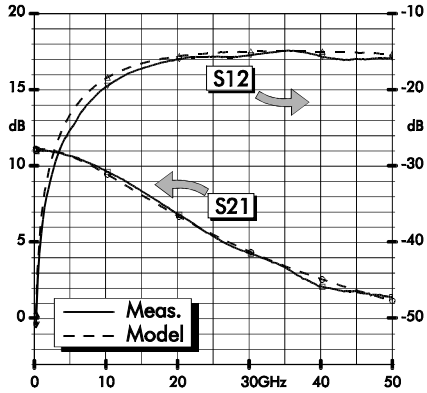

Fig.14: *comparison between measured and predicted [S] parameters of a T-shape 2x50µm biased at Vds=3V and Idss/2*

VI CONCLUSION

This paper describes an original concept of versatile FET modeling. The transistor metallic electrodes are separately modeled using an EM simulation. Active parts are described by an electrical equivalent scheme identical for each finger. This new model shows a very good agreement with FET measurements but it is also able to accurately predict new transistor response, without any geometrical restriction, from any single transistor sample. This seems to be a significant and valuable progress for MMIC design.

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